BENEFITS AND LESSONS LEARNED FROM THE USE OF THE COMPACT PCI STANDARD FOR SPACECRAFT AVIONICS

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Abstract

MESSENGER (MErcury Surface, Space ENvironment, GEochemistry, and Ranging) is a mission to orbit and explore the planet Mercury. MESSENGER will carry out comprehensive measurements for one Earth-year. The subsystem that controls the MESSENGER spacecraft is called the Integrated Electronics Module (IEM).

The IEM will operate the MESSENGER spacecraft, store data, and autonomously detect and mitigate onboard faults. In addition to meeting challenging requirements, the IEM must be available for integration on the spacecraft only 18 months after the start of full engineering development. The adoption of the 6U compact PCI (cPCI) standard has simplified the IEM development effort, reducing the time and cost that would otherwise be required. The 6U cPCI standard dictates board dimensions and the backplane electrical interface. The use of the standard has allowed some of the IEM boards to be specified and procured with a competitive selection process in a minimal amount of time. Prototype IEM systems have been assembled using commercially available backplanes, card racks, and Ethernet cards. Low-cost off-the-shelf cPCI tools such as board extenders and bus analyzers have been used to aid development. These components and tools would have to be developed at a significant cost if a proprietary or non-commercial board format had been adopted. The 6U cPCI specification itself does not address board level mechanical and thermal requirements, but features were added to the boards to meet these requirements while retaining compatibility with the cPCI standard. This paper details the benefits and lessons learned that have resulted from the use of the 6U cPCI standard in the development of spacecraft avionics.

Introduction

MESSENGER (MErcury Surface, Space ENvironment, GEochemistry, and Ranging) is a mission to orbit and explore the planet Mercury [1]. The mission plan is to launch in March 2004 and use two flybys each of Venus (June 2004 and March 2006) and Mercury (July 2007 and April 2008) to arrive at Mercury in April 2009 [2]. MESSENGER will orbit Mercury and carry out comprehensive measurements for one Earth-year. The subsystem that will control the MESSENGER spacecraft is called the Integrated Electronics Module (IEM). The IEM will operate the spacecraft, store data, and autonomously detect and mitigate onboard faults.

IEM Design

The Johns Hopkins University Applied Physics Laboratory (JHU/APL) started preliminary design of the MESSENGER mission in early 2000. The preliminary design of the IEM was completed by the end of that year. Design considerations included:

- The schedule was short; only 18 months were available from the start of full engineering development to delivery of first flight IEM.
- Previous JHU/APL IEM designs did not offer sufficient computational throughput or data storage, so new designs were necessary.

Based on these considerations, it was decided that the IEM design should leverage as much as possible off work already performed in industry instead of pursuing in-house custom designs to meet the program requirements. In order to

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accelerate the schedule and minimize costs, it was decided to base the design on the 6U compact Peripheral Component Interconnect (cPCI) standard. This choice greatly aided the preparation of board level specifications and maximized the use of commercial off-the-shelf (COTS) components. The use of COTS components is advantageous because the number of custom items that must be developed (at a significant cost) is reduced. It was recognized that the 6U cPCI board format was not optimal from a mechanical and thermal standpoint for spacecraft use, but it was believed to be "good enough." Conductive heat sinks and board stiffeners could be used to satisfy mechanical and thermal requirements and retain 6U cPCI compatibility.

At the conclusion of the preliminary design phase, the IEM design was partitioned into five daughter cards, a backplane, and a cast aluminum chassis. A block diagram of the IEM is shown in Figure 1. Three of the five daughter cards communicate over a PCI bus. Three of the cards (Main Processor, Fault Protection Processor, and Solid State Recorder) were designed and manufactured by BAE SYSTEMS to JHU/APL specifications. These boards were specified to be as generic as possible, incorporating few features that would be mission unique so that they could be easily specified and used on multiple spacecraft programs. The Main Processor (MP) and Fault Protection Processor (FPP) boards are nearly identical. The Interface Board and Converter Board were designed and built by JHU/APL. These boards capture the MESSENGER-unique requirements. The chassis and motherboard were designed by JHU/APL and fabricated out of house.

The three breadboard IEM systems were built to maximize the amount of COTS components so they could be produced as rapidly as possible. The two flight IEM systems have mechanical and thermal requirements that necessitate custom built (not COTS) boards and chassis.

Board Format Selection Considerations

Three card formats were initially considered for the IEM: Extended SEM-E (formally known as IEEE-1101.7-1995), 3U cPCI, and 6U cPCI. The Extended SEM-E format was considered because

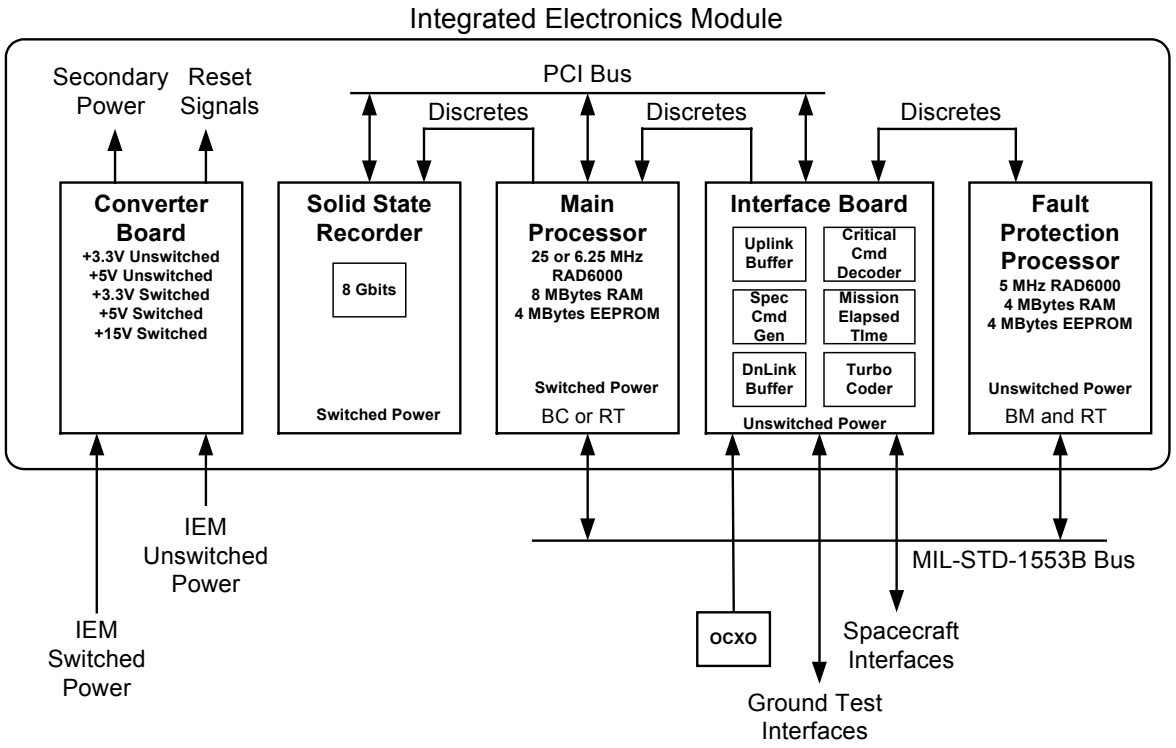

Figure 1. MESSENGER Integrated Electronics Module Block Diagram

JHU/APL had used it for the previous generation of IEM, and it has good mechanical and thermal design features for space avionics use. The cPCI standards are beginning to be used in space applications; the Jet Propulsion Laboratory X2000 program is using the 3U cPCI format, and the Langley Research Center-managed GIFTS spacecraft is using the 6U cPCI format. The 3U and 6U cPCI cards have the same depth (160 mm), but the 6U format is taller (233.35 mm) than the 3U format (100 mm).

The 6U card is almost identical to the Extended SEM-E in overall board area (length times width). *Effective* board area is the area available for application electronics; it is the area left after subtracting out area needed for backplane connectors, stiffeners, card locks, and backplane interface circuitry. As seen in Table 1, the 6U format is slightly more efficient than the Extended SEM-E format in terms of effective board area and board area per board weight. The implication is that more circuitry can fit on a 6U board than an Extended SEM-E board, at a lower weight. The 6U format, with some of the modifications for spacecraft avionics use, is shown in Figure 2. Two of the backplane connectors are shown removed (discussed in a later section), and wedgelocks are added to clamp the board into the flight chassis.

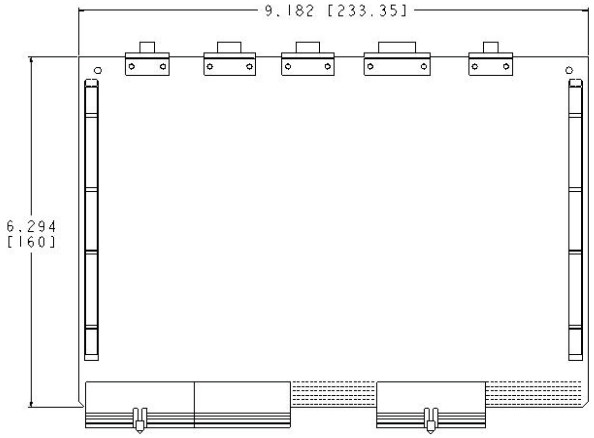

Figure 2. 6U cPCI Board Format

Table 1. IEM Board Format Selection Criteria

Parameter	Extended SEM-E	3U cPCI	6U cPCI
Area (one side, cm^2)	364	157	366
Effective Board Area = Total Board area – card locks – backplane connectors - backplane I/F circuitry ($cm^{2)}$	594	235	677
Effective board compared to desired functional blocks	Close Match	Too small	Close match
Board edge length available for I/O connectors (cm)	13.6	8.1	21.3
Weight (g)	467 to 953 (TIMED S/C actual weights)	No data	526 – 998 (MESS. estimates)
Effective board area per lb (cm^2/g)	0.62 – 1.27	No data	0.68 – 1.29
Thermal Conductivity (rank, 1=best)	1	2	3
COTS equipment readily available	No	Yes	Yes
Number of boards on PCI Bus (fewer is better)	3	9	3
Overall Development Cost (rank, 1= best)	3 (all custom)	3 (need 2x–3x the number of cards)	1 (minimize # of boards, maximize use of COTS)

Test equipment (cPCI backplane analyzers and card extenders), prototyping equipment (chassis and backplanes), and boards useful during development (Ethernet cards and bridge boards) are significantly cheaper with the 6U approach than with an Extended SEM-E approach. They are available off the shelf instead of needing to go through a design-fabricate-assemble-test cycle.

The basic stand-alone building blocks in the IEM are the five boards: (1) MP, (2) FPP, (3) Solid State Recorder (SSR), (4) Interface, and (5) DC/DC Converter boards. All boards are tightly packed; the MP, FPP, and SSR make use of stacked components in order to fit all desired functions on the board. There is little wasted space. Photos of MP and SSR engineering model boards are shown in Figures 3 and 4. The ratio of effective board area between the 6U and 3U formats is 677/235 = 2.9. This means that each densely packed 6U board would need to be replaced with three 3U cards. If the boards were less densely packed, so that only one or two 3U boards were required to replace a single 6U card, the 3U format would be more attractive. But based on the board layouts, the five 6U boards in the IEM would have to be replaced by about fifteen 3U boards. An approach using 3U boards would be more costly, since designing and fabricating three 3U boards would be more expensive than a single 6U board.

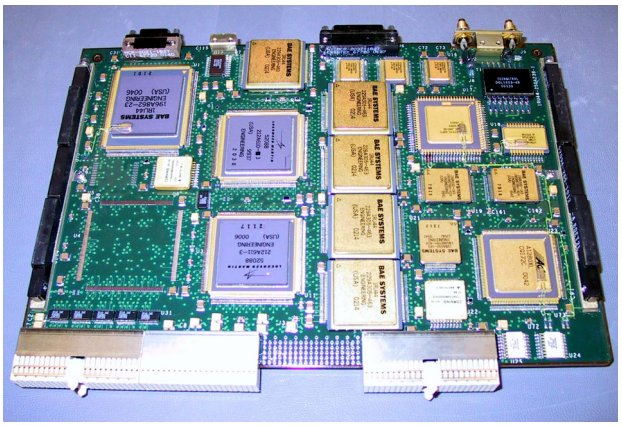

Figure 3. IEM Main Processor Board

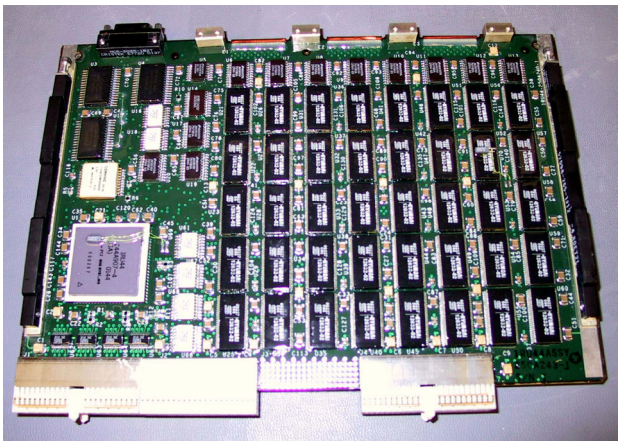

Figure 4. IEM Solid State Recorder Board

Another consideration in selecting the 6U format over the 3U format is the number of IEM boards connected to the PCI backplane bus. If the 3U format were used, nine boards would have to be connected to the PCI bus. However, the cPCI specification only allows a maximum of eight boards to operate on a single backplane. For this reason there would be a significant technical risk in achieving proper function with a system having nine boards on the PCI bus. It might be necessary to break the PCI backplane bus into two or more segments. This would require the addition of PCI bridge chips to the design, a significant complication.

For a variety of reasons the decision was made to contract out the MP, FPP, and SSR boards. Radiation-hardened, high-performance processors were only obtainable from processor vendors as boards, not chips. There were no existing processor or SSR boards available that could meet the MESSENGER requirements; specifications had to be written and a competitive bid process followed. By using commercial standards as much as possible, the time required to write the specifications was minimized, because most of the backplane bus and card dimension sections could simply refer to the cPCI specification. The cPCI standard was thus preferred to the Extended SEM-E format, which is not as widely used and does not include a backplane bus definition.

The major drawback of the 6U format is that it is more difficult to conduct heat off the board than the other standards. This is because the board makes contact with the chassis along the shorter

160 mm board edge rather than the longer 233.35 mm edge. Spacecraft avionics rely primarily on conduction to remove heat, so the lesser the contact area between the board and chassis, the more difficult it is to conduct heat off the board. However, thermal analyses have shown that thermal de-rating criteria will be met even for the hottest board.

In summary, the 6U format was selected over the Extended SEM-E format because it is somewhat more efficient in effective board area and lower in weight per board area. It is lower in overall cost due to the availability of low-cost COTS equipment, and saves time because the equipment can be bought off the shelf instead of being developed with a design-fabricate-assemble-test cycle. Also, specifications for 6U boards can be written more quickly than those using the Extended SEM-E format. The 6U format was selected over the 3U format because as many as fifteen 3U cards would be required in place of the five 6U cards. This number of cards would add cost and technical risk.

PCI Chip Selection

Within the MESSENGER IEM there are three boards connected to the PCI bus. Of these, the RAD6000 chipset on the Main Processor board and the Power PCI Bridge chip on Solid State Recorder board have inherent PCI capability. The JHU/APL designed Interface board is the third board on the PCI bus. Several PCI interface implementations were considered: an Actel PCI core in an Actel radiation-tolerant Field Programmable Gate Array (FPGA), and several chips with PCI interfaces available from BAE SYSTEMS. It was decided that the lowest-risk approach was to select the most appropriate PCI chip from BAE SYSTEMS.

This approach had several advantages. First, since an existing chip has a fully defined backend, the development of the Interface board could begin almost immediately. Second, it greatly increased the likelihood that all of the components on the PCI bus would operate together properly, since they would all come from a common source (BAE SYSTEMS). After reviewing the available chip designs, the PHASOR (**P**ower **H**andling, with **A**ccess to **S**ummit and **O**ptical bus **R**esources) chip was selected. This chip has a 16-bit back end bus, which minimized the amount of hardware needed on the board, compared to a 32-bit bus. The data throughput of the chip was low but adequate for the bandwidth required by the MESSENGER mission.

The PHASOR chip also has the advantage of having Input/Output (I/O) that is tolerant of voltages higher than the 3.3 V that powers the chip. The PHASOR chip is on a switched 3.3 V DC/DC converter, and the rest of the board is on an unswitched 3.3 V DC/DC converter. The high-voltage-tolerant I/O on the PHASOR chip made it possible to connect together chips powered from different supplies.

Lessons Learned with COTS Equipment used for IEM Breadboard Development

Backplanes and Enclosures

Standard cPCI backplanes and enclosures were used for the IEM breadboards, but in a unique configuration three independent backplanes were installed in a single enclosure. Bustronic was selected to supply these backplanes and enclosures. Two four-slot and one six-slot backplanes were used. Separate backplanes were required because some of the IEM boards operate on switched power while others operate on unswitched power. An IEM breadboard is shown in Figure 5.

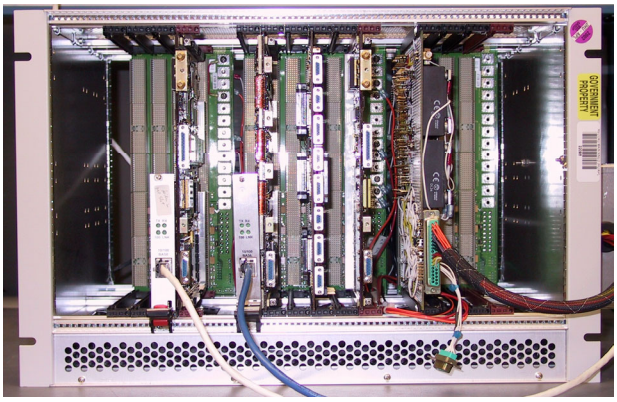

Figure 5. Front of IEM Breadboard

Backplanes compliant to PICMG 2.0, Rev. 3.0 were desired, because these have independent clock lines from the system slot board to each peripheral board. The older cPCI specification is less robust because two peripheral slots each share a single clock line. The MP board functions as the cPCI system slot board. System slot boards are required

to have seven PCI clock signal outputs. Because the MP supports only five clock outputs, the backplane manufacturer had to be contacted to determine how the clock outputs are routed to the peripheral slots inasmuch as this is not specified by cPCI. Only the peripheral slots that have clock lines routed to them from the MP can be used.

Extender Cards

Extender cards are needed during the development of cPCI boards for debugging purposes. While not guaranteed to work (they violate cPCI track-length requirements), it was found that a cPCI passive extender worked, up to the 25-MHz PCI clock frequency used in the IEM design. Numerous cPCI passive extenders were available; an extender from Catalyst Enterprises (P/N 6U-CPCI) was selected because it had the simplest electrical design. Many extenders included switches that permitted each cPCI signal to be individually disconnected from the board. It was felt that the simplest design, with the fewest disturbances to the PCI signals, offered the best chance of success.

Since the J3 and J5 backplane connectors are not used in the IEM design, the extenders were ordered with those connectors depopulated in order to minimize the insertion and extraction forces of the extender in the chassis. A downside of the extender is that there is no easy way to extract it. The extender used is shown in Figure 6.

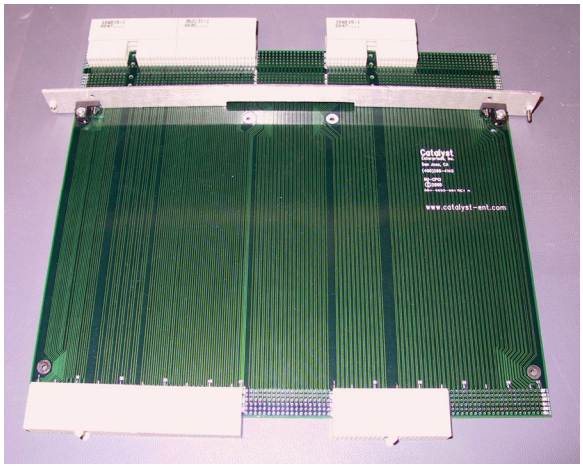

Figure 6. 6U cPCI Extender Card

Ethernet Card

CP610/1 Ethernet cards from RAMIX were used in the IEM breadboards to support software development. The RAD6000 processors are designed so that the PCI clock rate equals the processor clock rate, so that when the processor is at a low clock rate, the PCI clock is at the same low rate. A problem was found when the RAD6000 processors were operated at 5 MHz (FPP) and 6.25 MHz (MP in one mode). The Ethernet cards would not operate properly when connected to the Ethernet network switch. The problem was found to be that the Ethernet cards would auto-negotiate with the switch to 100-Mb/s operation but could not actually operate at 100-Mb/s at low PCI clock rates. The solution was to place a fixed rate 10 Mb/s hub between the Ethernet cards in the IEM and network switch. Another potential solution would be to change the driver for the Ethernet card so that it forced operation at 10-Mb/s. The Ethernet cards also required a modification to operate without +/- 12 V supplies, since the IEM operates from +3.3 V and +5 V only.

Bus Analyzer

A cPCI bus analyzer from VMETRO, Inc., was used during the development of the IEM. It operated successfully with RAD6000 processor boards.

Rear Transition Card

6U cPCI has five backplane connectors designated J1-J5. The use of the J1 and J2 connectors is reserved by the cPCI specification. The J3-J5 connectors are undesignated and available for use. On the IEM, J3 and J5 are depopulated to minimize insertion and extraction forces, and all unique signals on the backplane are routed on the J4 connector. The cPCI specification defines rear transition cards that can plug into the back of standard cPCI chassis to make connections to the J3-J5 connectors of each cPCI card. However, no COTS rear transition cards were found that would allow connections to be made from one rear transition card to another, so a custom rear transition card was designed and fabricated. The cards are used to make all of the inter-board connections that are unique to the IEM. Figure 7 shows an individual rear transition card and

Figure 8 shows the back of a breadboard IEM with the wiring harness used to make these connections. Because all of the signals are low speed, controlled impedance connections were not needed.

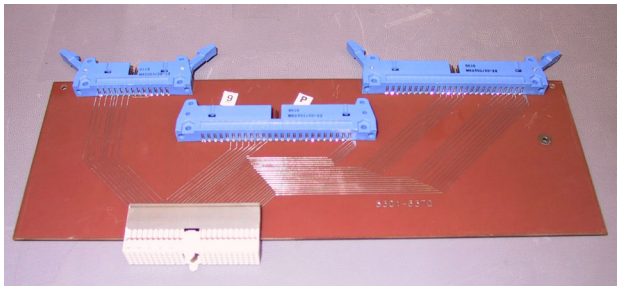

Figure 7. Rear Transition Card

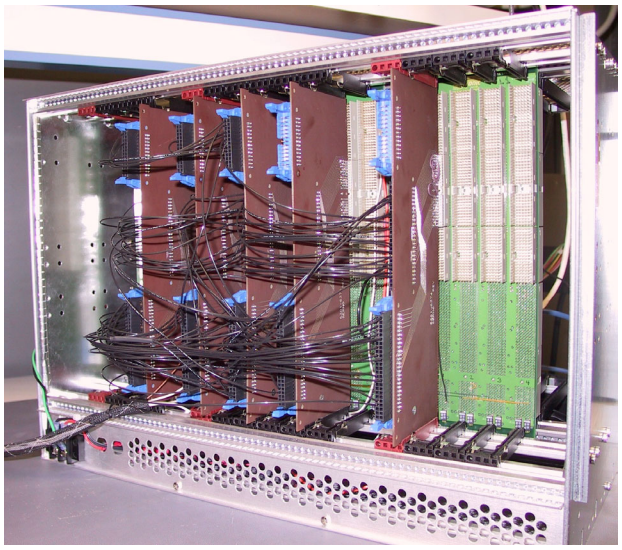

Figure 8. Rear of IEM Breadboard Showing Rear Transition Card Wiring Harness

Lessons Learned with COTS Equipment Used for IEM Interface Board Development

An advantage of adhering to a commercial standard for the IEM boards is that COTS equipment can be used to test the boards. An Interface Board Test System (IBTS) was built to test the IEM Interface board. It employed an open-ended cPCI chassis from Tracewell Systems (Figure 9.). To reduce cost and development time, a standard desktop PC with a PCI-to-cPCI bridge was used as a system slot board rather than using a standalone cPCI processor board (RAD6000 or otherwise). A PC to cPCI board from SBS Technologies was selected. Microsoft Visual C++ and Venturcom Real Time Extensions (RTX) were utilized to develop the software to control the Interface Board.

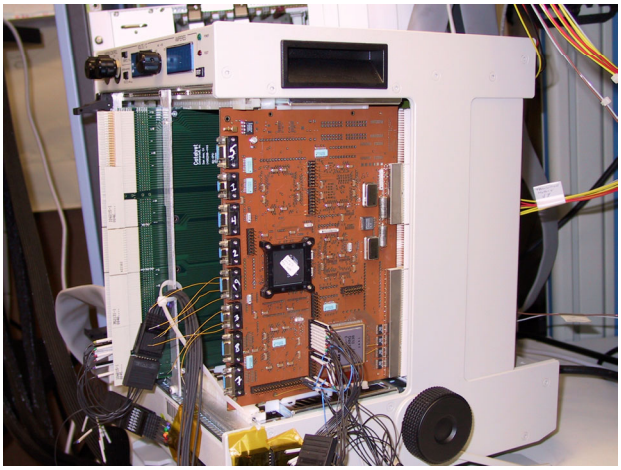

Figure 9. IEM Interface Breadboard in Test Chassis

One difference encountered by using a PC with a bridge board rather than a RAD6000 processor board is that a PC has a fixed PCI clock rate of 33 MHz. This is faster than the PCI clock rate in the IEM (25 MHz). So, if a PC is used to drive the system slot in the cPCI backplane, the developer should verify that the PCI chip on the board under test can support operation at 33 MHz even if it is operated at a lower rate in the final configuration.

PHASOR Chip PCI Configuration Problem

Trouble arose when it was found that the PHASOR chip used on the Interface board, while fully PCI compatible, was not fully compatible with the Basic Input/Output System (BIOS) found in Wintel PCs. The difficulty arose because the PHASOR chip maps its Optical Bus Interface (OBI) into I/O space and requests 32 MB of space. While this is well within the allowed limits of the PCI specification (which allows up to 2 GB of IO space), it far exceeds the maximum IO size allowed by the BIOS in a Wintel PC. The maximum available on a Wintel PC is only 64 kB. The amount available to non-system devices is even less, since all addresses below 0x3FF are reserved.

This problem presents itself immediately upon boot-up of the host computer. During boot-up, the Wintel BIOS configures the PCI devices by querying them for their memory and IO space needs, and then setting their Base Address Registers (BARs) accordingly. When the BIOS attempts to configure the PHASOR chip, it realizes that BAR1 (the OBI IO Base Address Register) is requesting 32 MB of IO space. Since this amount is not available, BIOS detects a failed configuration, and reports the following error:

Plug and Play Configuration Error

Strike the F1 key to continue, F2 to run the setup utility.

By striking the F1 key, the computer continues booting up. Unfortunately, the PHASOR chip is left in a state where both PCI IO and memory accesses are turned off.

Although this problem was difficult to diagnose, the solution is rather straightforward. By performing a configuration cycle on the PHASOR chip, the BAR1 can be moved out of the PC's IO space and into an innocuous location. The software product Real Time Extensions (RTX) was used to perform the configuration read and write operations. RTX "provides an essential set of real-time programming interfaces in the Win32 environment." In this circumstance, RTX is particularly useful because it provides a function call that will do configuration accesses directly over the PCI bus under application software control.

Big Endian Versus Little Endian

Data stored in a byte addressable memory can be implemented as Big Endian or Little Endian. The PCI bus specifies Little Endian byte ordering in that the least significant byte is contained in bits AD[7:0] and the most significant byte is contained in bits AD[31:24]. Only the first 64 bytes of the PCI configuration space for a given PCI device is specified as Little Endian. RAD6000 devices are generally Big Endian, which reverses the bytes compared to Little Endian. This became an issue when accessing the PHASOR chip using a PC. While the PCI configuration space was as expected (Little Endian), byte swapping must be performed for the other registers, relative to how they are defined in the PHASOR specification. This will be the case for many of the PCI chips developed by BAE SYSTEMS when connected to a non-RAD6000 (Little Endian) processor.

Interrupt Processing

The PHASOR chip interrupt processing was not as straightforward as hoped, although the configuration cycle problem was certainly more difficult to solve. The PHASOR did not implement the Interrupt Pin and Interrupt Line registers in the PCI configuration header. The software therefore could not query the configuration space and find out the interrupt vector from the PHASOR itself. The cPCI standard assigns interrupts based on logical board slots. The same board will drive one of four different interrupt pins based on its position in the backplane. It was not clear what interrupt the PHASOR was driving in the cPCI chassis. This was solved by using the VMETRO cPCI Bus Analyzer to discover which interrupt was driven by the PHASOR for each slot and then attaching and enabling interrupts based on that knowledge. The test software needed access to the Hardware Abstraction Layer (HAL) interrupt API to attach interrupts manually. The solution used RTX, which allowed interrupts to be attached and enabled within Windows.

The interrupt processing itself was straightforward. Windows uses the thread-interrupt model instead of traditional interrupts. RTX provided several ways of installing interrupts and also generating a process to respond to them. The simplest and slowest method was used. A worst-case interrupt latency of less than 2 ms was observed using Windows NT 4.0. With additional effort this performance could be improved but this was sufficient for this application.

Deviations from the cPCI Specification

In some cases, requirements in the cPCI specification could not be followed or were intentionally not followed. The first class of these deviations is due to limitations of the RAD6000 processor. The RAD6000 was designed before the cPCI specification was established. In some areas the RAD6000 deviates from the cPCI specification,

and modifications must be made to COTS equipment in order to work with the RAD6000.

Number of PCI Clocks on System Slot Board

The RAD6000 chipset supports seven PCI clock outputs. Since two are used on the processor board, only five are available for use off card. The cPCI specification requires the system slot board to have seven clock outputs (one per peripheral slot). Because only five are available, the user must check with the backplane vendor to determine which peripheral slots will be connected to the available clock outputs, since the assignment of PCI clock outputs to peripheral boards is not made in the specification.

Number of Bus REQ/GNT Signals on System Slot Board

The RAD6000 chipset supports five PCI Bus Request/Bus Grant signal pairs. Two of the pairs are used on the processor board. Three are available for use off card. The cPCI specification requires the system slot board to have seven signal pairs (one per peripheral slot). Since only three signal pairs are available, only three peripheral boards can be PCI bus masters, which make use of these signals to request use of the bus. The user must assign peripherals cards with bus master capability to those slots, or modify the backplane so that slots that need the signals have jumpers to slots that have them but don't use them. These modifications were made to the IEM breadboard backplanes.

Different AD Signals Used for ID Select

The cPCI specification calls out the use of ID Select (IDSEL) signals to provide unique access to each slot for configuration purposes. This is done by tying a unique AD signal to the IDSEL pin at each slot on the backplane. During configuration cycles, a device is selected for configuration by driving its IDSEL signal active. The cPCI specification specifies that AD[31:25] be used for this purpose. However, the RAD6000 uses the signals AD[18:11] instead. In order for PCI configuration cycles to work with a RAD6000, commercial backplanes must be modified. At each peripheral slot, the IDSEL pin must be isolated, and a jumper wire must be added between the IDSEL pin and an AD pin that is driven by the RAD6000 during PCI configuration.

Deletion of P3 and P5 Connectors

6U cPCI requires the presence of five backplane connectors, designated J1-J5. The use of J1 and J2 is reserved. J3, J4, and J5 are user defined. J4 is used for all of the IEM-unique I/O signals. J3 and J5 are not installed on the boards in order to reduce insertion and extraction forces. Testing has shown that the J3 and J5 are not needed to provide mechanical support when the IEM is vibrated to simulate launch conditions.

Board Envelope and Spacing

The IEM boards are cPCI compliant for card length and width, but they are not compliant in regards to card thickness. cPCI systems have a board spacing of 20.32 mm inches. In addition, cPCI boards are defined as having components installed on one side only. The IEM boards violate the thickness standard because they have components on both sides. In order to use commercial backplanes in the breadboard IEM, the slots on either side of some IEM breadboards are left empty. The flight IEM is designed with a board spacing of 26.82 mm to accommodate the thicker boards.

Box Cover Instead of Board Front Panels

The cPCI specification requires the use of a front panel with handles on each board. The IEM boards were designed without individual front panels. Instead, the flight model IEM has a single front cover with cutouts for the connectors on each board. This was done for several reasons. First, it was assumed that the cPCI specified board spacing of 20.32 mm could not be adhered to. So, when the specifications were written for the boards, the board spacing was not known and the front panel width could not be specified at that point. Instead, the cover was designed after the board spacing was determined. Second, the flight chassis would not be designed like a commercial cPCI enclosure due to the additional mechanical and thermal constraints it must satisfy. Until the flight chassis was designed, it was not clear how the front panels (if used) would

be attached to the chassis. So, the front panel design could not be included in the board specifications. Third, a single integral cover provides better mechanical support than individual front panels. Fourth, a single front cover will weigh less than individual front panels with handles. The flight IEM design with attached cover is shown in Figure 10.

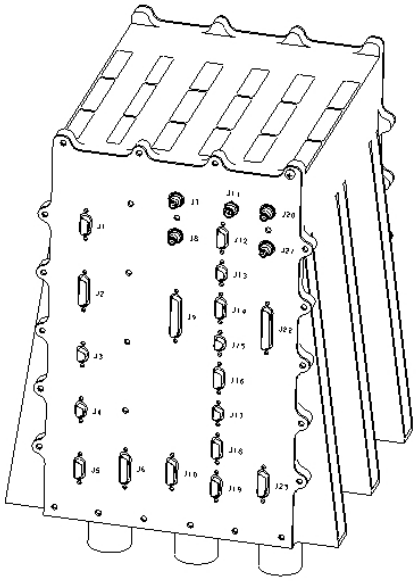

Figure 10. Flight IEM Design

Instead of using the ejectors normally found on the front panel of cPCI boards, holes were included in the top and bottom front edge of the cards. An ejector tool is used to engage the holes and remove the boards from the chassis (both the commercial breadboard chassis and custom flight chassis). The ejector was modified to accommodate the thicker boards.

Length of AD Traces on System Slot Board

The final deviation from the cPCI specification is the length of the PCI bus signal traces on the MP and FPP boards. The actual PCI signal stub lengths exceed the 63.50 mm length called out in the specification. This is mitigated by reducing the maximum PCI clock to 25 MHz and by restricting the PCI signal loading in the flight configuration to three boards.

Conclusion

Three IEM breadboard systems have been assembled using 6U cPCI COTS components, one year after the start of full engineering development on the MESSENGER program. The breadboard IEMs were designed, fabricated, and assembled approximately six to twelve months faster than if a full custom, non-COTS approach had been taken. In addition, this design approach had other benefits that could not be easily achieved in a custom non-COTS design, such as the availability of Ethernet cards and bus analyzers. The schedule and cost benefits of a COTS-based design more than offset the non-optimal mechanical and thermal aspects of 6U cPCI that required mitigation.

There are a couple of cautionary notes. Simply because a COTS-based design is used does not mean that the design does not have to be understood in depth. System design decisions and tradeoffs still have to be made. Also, while it may be most effective to procure boards in some cases, visibility of board-level operations can be lost. This loss can be significant, since design decisions made at the board level can have significant system-level implications.

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