A LIGHTWEIGHT INTEGRATED ELECTRONICS MODULE (IEM) PACKAGING DESIGN FOR THE MESSENGER SPACECRAFT

Sharon X. Ling, Richard F. Conde, and Binh Q. Le

Johns Hopkins University Applied Physics Laboratory

Laurel, MD 20723-6099

Abstract

MESSENGER (MErcury Surface, Space ENvironment, GEochemistry, and Ranging) is a mission to orbit the planet Mercury. The comprehensive scientific data collected through the one-Earth-year orbital mission phase will allow scientists to study and understand the environment and evolution of the innermost terrestrial planet. The five-year cruise phase and the harsh environment of Mercury orbit pose challenges to the spacecraft subsystem design in terms of balancing an extremely tight mass budget with robust thermal and mechanical designs. The packaging design for a low-cost, lightweight Integrated Electronics Module (IEM) is presented in this paper. The commercial 6U Compact Peripheral Component Interconnect (PCI) Printed Wiring Board (PWB) design has been selected to reduce development cost. Several unique features of the IEM packaging design include using the RAD6000 processor developed by BAE Systems in the Main Processor board, 64-Mb Hyundai TSOPs stacked two-high for 1 GB of SDRAM on the Solid-State Recorder Assembly, and a 32-mm Ceramic Column Grid Array as the PCI Bridge chip. The IEM chassis that accommodates five PWBs is designed with thin-wall aluminum for weight savings, and is fabricated by investment casting for cost savings. Extensive thermal and structural analyses have been performed to ensure that the IEM is capable of surviving and functioning during launch, cruise, and orbit. Environment tests have been conducted on the pre-engineering IEM to validate analytical results.

Introduction

MESSENGER is the first spacecraft that will orbit the planet Mercury [1]. The mission design has provided two launch windows, with a primary window in March 2004 and a secondary window in May 2002 [2]. The spacecraft will be commanded to perform two deep space maneuvers, two Venus flybys, and two Mercury flybys during its long cruise phase, and will be inserted into Mercury orbit in April 2009. The spacecraft will then orbit Mercury for the one-year mission with an 80° inclination in a 12-hour period and periapsis latitude and elevation of 60° N and 200 km, respectively. Science data will be collected by a suite of onboard instruments that include the Mercury Dual Imaging System (MDIS), the Mercury Atmospheric and Surface Composition Spectrometer (MASCS), the Gamma-Ray and Neutron Spectrometer (GRNS), the X-Ray Spectrometer (XRS), the Magnetometer (MAG), the Mercury Laser Altimeter (MLA), and the Energetic Particle and Plasma Spectrometer (EPPS) [3].

The Integrated Electronics Module (IEM) as shown in Figure 1 is the central control element for the entire spacecraft. There are two IEMs onboard the spacecraft for redundancy. Each IEM accommodates five Printed Wiring Boards (PWBs). These as shown in Figure 1, in order from left to right, are the DC-DC power converter board, the Solid State Recorder (SSR) board, the Main Processor (MP) board, the interface board, and the Fault Protection Processor (FPP) board. The five PWBs are plugged to a motherboard that is not shown in the figure.

The tight mass budget, severe thermal environment, and unique construction of the composite spacecraft have posed many challenges to IEM design. Extensive analyses and testing have been conducted to ensure the functionality and the thermal and structural integrity of the IEM through the entire mission.

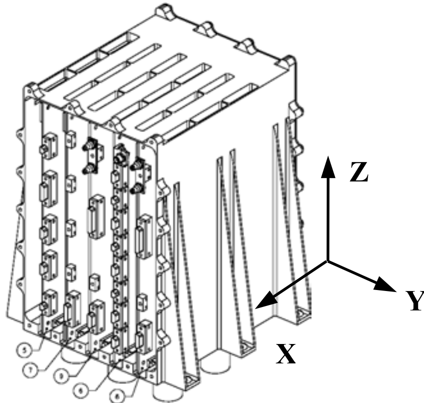

Figure 1: The MESSENGER IEM

MESSENGER IEM Design

The MESSENGER IEM has several unique features. The commercial Compact PCI 6U form factor has been chosen so that commercial off-the-shell test equipment and software can be readily available for testing. The thin-wall aluminum investment casted chassis is designed for weight saving and cost reduction. The entire IEM module weighs only 5.871 kg, a 40% reduction in weight compared to similar systems on previous missions. Thermal vias are used to conduct heat to a heatpipe under the composite deck. Slip joints are designed to accommodate the Coefficient of Thermal Expansion (CTE) mismatch between the composite structure and the aluminum chassis to eliminate potential structural damage.

IEM PWB Design

Compact PCI 6U form-factor, multi-layer polyimide printed wiring boards are used in the IEM design. The Compact PCI standard has been chosen for cost saving. There are five PWBs in each IEM chassis. The PWBs are connected to the sixth PWB, a motherboard, through Compact PCI backplane press-fitting connectors and are secured inside the chassis using board-mounted wedgelocks to save space. The construction of each board varies with the thermal and structural requirements.

MP and FPP Boards

The MP and FPP share the same board design, except that the heatsink plate for the RAD6000/LIO 6001 is not employed for the FPP board. The FPP board operates at a lower processor speed and generates less power; therefore, no additional heatsink is needed. Figure 2 and Figure 3 show the front and backside of the PWB layout for the MP and FPP boards. Each PWB utilizes a 16-layer double-sided PWB with blind vias and an AlBeMet rib to enhance structural stiffness. The board thickness is 2.79 mm (0.110 in). The PWBs are being built per IPC-6012, class 3, at Lockheed Martin's facility at Owego, NY.

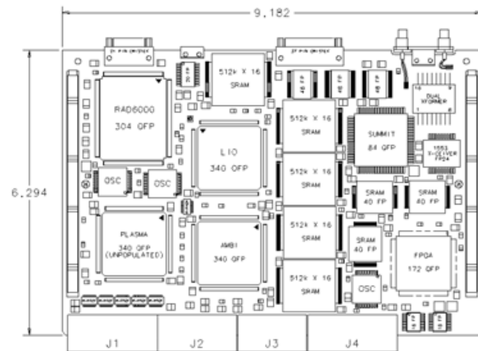

Figure 2: Front side of the MP and FPP Boards

Figure 3: Backside of the MP and FPP Boards (the heatsink is used only for the MP Board)

SSR Board

The SSR PWB is also being built at Lockheed Martin's facility. The SSR board is constructed by two single sided, 12-layer PWBs sandwiched by an aluminum plate (2.79 mm thickness), as shown in Figure 4 and Figure 5. The plastic SDRAMs are populated on both sides of the PWB. The aluminum plate is used as a heatsink to control the junction temperature of the plastic components, which, after derating, is 85°C. The total board thickness of the SSR is 6.70 mm (0.264 in).

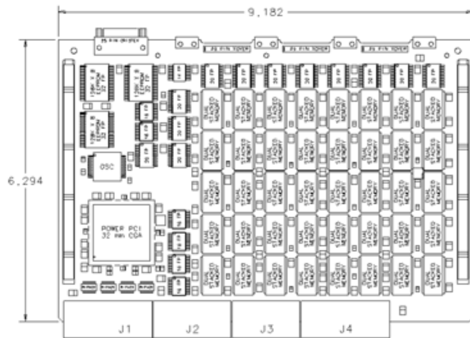

Figure 4: Front Side of the SSR Board

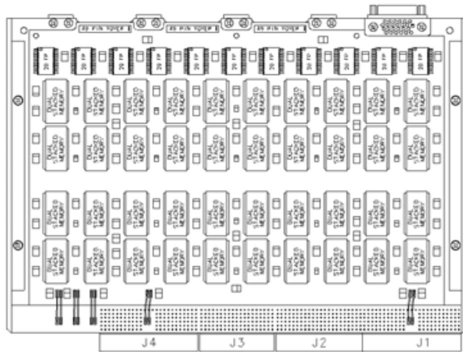

Figure 5: Backside of the SSR Board

Interface Board

The interface board is a 10-layer PWB and has been designed and built at The Johns Hopkins University Applied Physics Laboratory (JHU/APL), per MIL-5510F, type 3. Figures 6 and 7 show the front and the backside of the interface board design. The board thickness is 1.57 mm (0.062 in). An aluminum stiffener is used to increase the board stiffness.

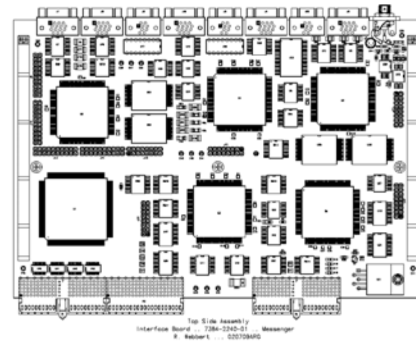

Figure 6: Front Side of the Interface Board

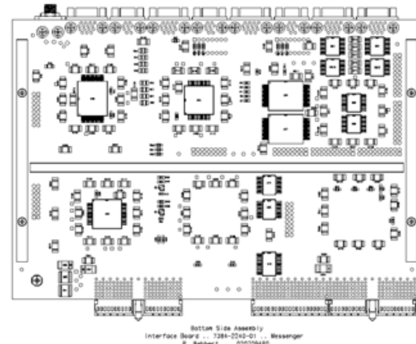

Figure 7: Backside of the Interface Board

DC-DC Converter Board

The DC-DC converter board is also a 10-layer PWB that will be fabricated at JHU/APL. An AlBeMet heatsink plate (2.03 mm) is designed to provide adequate stiffness of the board that accommodates large converters, as well as sufficient heat dissipation path from the converters to the chassis. Figure 8 and Figure 9 are layouts of the front and backside of the DC-DC converter board. The heatsink plate is bonded to the secondary side of the PWB using Thermabond, and the converters are mounted directly on the heatsink to enable maximum heat dissipation. The chassis design has been carefully reviewed to ensure sufficient spacing between the heatsink and the internal wall of the chassis to avoid mechanical interference during vibration. No stiffener is required in the DC-DC converter board design as the result of using the AlBeMet heatsink plate.

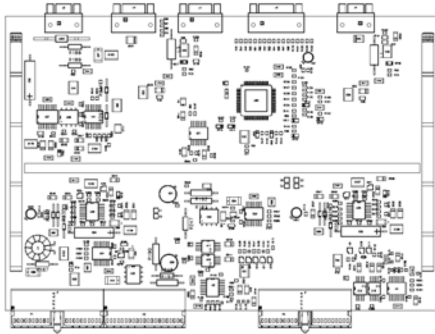

Figure 8: Front Side of the DC-DC Converter Board

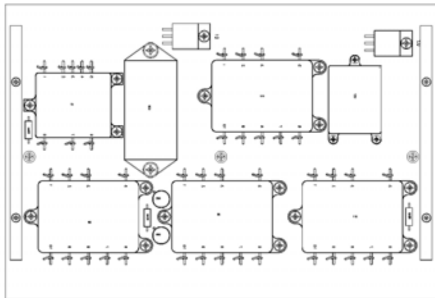

Figure 9: Backside of the DC-DC Converter Board

Motherboard

The motherboard of the IEM has been designed at JHU/APL and will be fabricated at an external foundry. Four stiffeners are attached on the backside of the board, as shown in Figure 10. The stiffeners are also attached with the back cover of the chassis to enhance the motherboard stiffness during daughter card insertion.

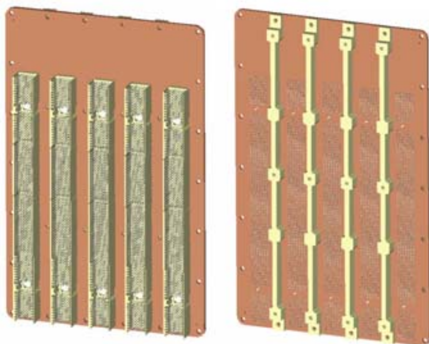

Figure 10: MESSENGER IEM motherboard

IEM Chassis Design with Thermal Vias

The IEM chassis is a thin-wall hulk casted using aluminum A-356 T6. The casting technique was chosen for cost savings, compared to the traditional hog-out method for flight chassis fabrication. The nominal wall thickness is 1.524 mm (0.060 in). The wedgelock retaining railings are built-in on the internal upper and bottom walls of the chassis. The front and back covers of the chassis are fabricated using magnesium sheet metal for further weight savings.

The main structure of the MESSENGER spacecraft is constructed of a composite material [2]. The lightweight composite spacecraft deck has low thermal conductivity and cannot dissipate the heat generated by the electronics in the IEM. Therefore an alternative heat dissipation passage must be adopted. Heat pipes connected to thermal radiators are attached to the thermal vias of the IEM chassis directly for thermal control. Figure 11 shows two photographs of the IEM pre-engineering chassis with integrated thermal vias at the bottom of the chassis.

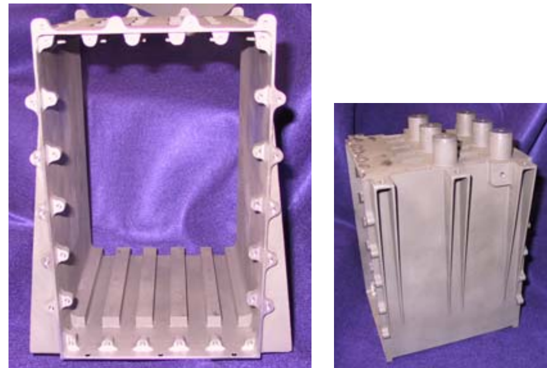

Figure 11: Aluminum Casted IEM Chassis

Slip-Joint Mounting of the IEM to the S/C

Another challenge posed by using the lightweight spacecraft composite structure is to accommodate the CTE mismatch between the electronic boxes, made of either aluminum or magnesium, and the composite deck. The concern of hard-mounting the electronic boxes directly to the composite deck is that thermal cycles during the orbital phase of the mission could exert excessive

force to the spool inserts, which could result in tearing or buckling of the thin compost face sheet.

The concept of slip-joint mounting is to use compliant mounting to absorb the CTE mismatch. The design approach utilizes four NEDOX-coated slip washers, two of which are located on each of the top and the bottom sides of the mounting bracket via spot faces, as shown schematically in Figure 12. The NEDOX-coated slip washers exhibit a reduced coefficient of friction, thus permitting relative displacement at the interface of the two slip washers to accommodate the CTE mismatch between the box and the mounting deck. The torque value for the IEM mounting is tailored to the size, weight, and location of the center of gravity (CG). The torque value needs to be high enough to prevent relative slippage during vibration while still accommodating slippage during temperature cycling.

The slip-joint design is still under development due to anomalies observed during the IEM pre-engineering vibration tests discussed in the next section. New tests of the coefficient of friction are underway, and modifications of the slip-washer coating material and thickness are expected.

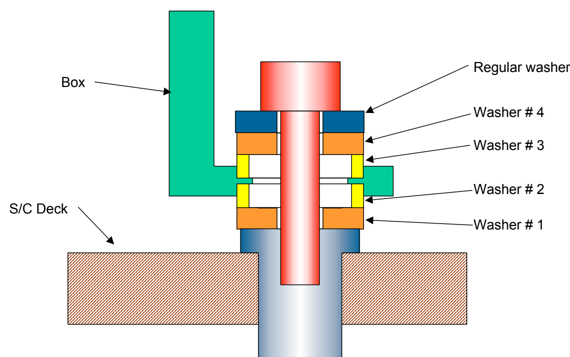

Figure 12: Schematic of Slip-Joint Mounting

MESSENGER IEM Thermal Design

The goal of the IEM thermal design is to ensure that the heat dissipation path can conduct 31.04 W, the maximum total IEM power through the thermal vias to the heatpipe, and that the junction temperatures of the components mounted on the five PWBs are below the derated values.

COSMOS /M 2.6 has been used to carry out finite element thermal analysis. Detailed procedures of the thermal analysis are described in the following sections.

Geometry

The IEM chassis is made of casted aluminum with a nominal wall thickness of 1.52 mm (0.060 in). The width of the chassis is 150.27 mm, the depth is 185.06 mm, and the height is 237.4 mm, without the mounting brackets and the thermal vias. The IEM chassis accommodates five PWBs, which connect to a motherboard through the Compact PCI backplane connectors. Two magnesium cover plates (1.52 mm) are designed to enclose the PWBs in the IEM.

Finite Element Model Generation

Thin-shell 4-noded elements have been used to model the PWBs and the chassis structure. The thermal conductivity of each board is calculated based on the board construction, including layer counts of the board, Cu weight on each layer, and heatsink material and thickness where applicable. The motherboard is not modeled in the thermal analysis, because there is no significant heat dissipated through the motherboard. The thermal resistance across the interface between the PWB and the chassis is not considered for ease of model generation. The worst-case power dissipation, as shown in Table 1, is used for the thermal analysis. The power dissipations are applied as discret nodal heat input based on the layout of the board.

The thermal vias are attached to the heatpipe plate on the opposite side of the composite deck from where the IEM is mounted. The heatpipe is attached to a radiator that will dissipate heat into deep space. Based on the spacecraft thermal model, the worst-case steady-state temperature at the heatpipe is 55°C. This temperature is used as the thermal boundary condition applied at the base of the thermal vias.

Table 1: Worst-case Power Dissipation of the IEM

	Power Dissipation (W)
Main Processor	7.30
Fault Protection Processor	3.20
SSR	4.00
OCXO (external of IEM)	2.25
Interface	3.32
Total Secondary Power	20.07
DC/DC Converter	10.97
Total IEM Primary Power	31.04

Thermal Analysis Results

Steady-state and transient thermal analyses were conducted for each PWB and for the entire IEM assembly.

Steady State Thermal Analysis Results

The steady-state PWB temperature distribution is calculated with the chassis finite element model. Junction temperatures are based on the thermal resistance from the board to the junction and the power dissipation of each component. The derating criteria [4,5] state that the junction temperature for silicon digital microcircuits should not exceed 100°C, or 15°C below the maximum allowable temperature, whichever is lower. This requirement limits the junction temperature to be no more than 100°C for all of the silicon devices on the IEM PWBs. Exceptions are for the RAD6000 processor on the MP board, for which the 105°C maximum tested temperature further restricted the junction temperature of the RAD6000 to be 90°C, and the SDRAMs on the SSR board, with derated junction temperatures of 85°C.

The temperature distribution (in K) for the chassis and boards is shown in Figure 13. The sidewalls of the chassis and the front and back covers are not shown. From the steady state board temperature distribution, junction temperatures are calculated. The current thermal design with thermal vias is sufficient to meet all junction temperature requirements.

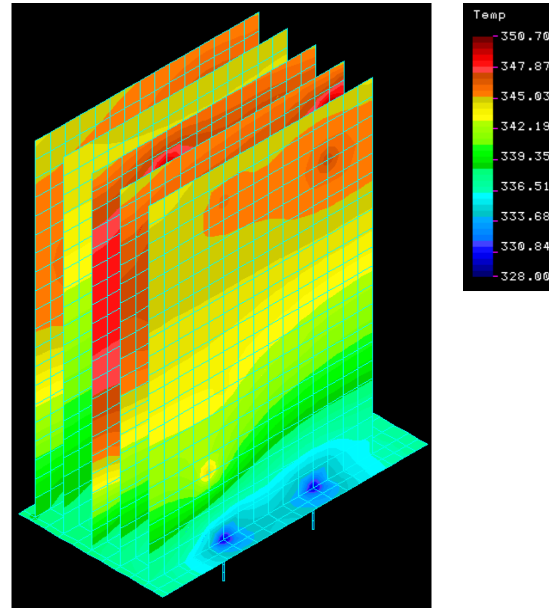

Figure 13: Steady-State Temperature (in K) for Thermal Analysis

Transient Thermal Analysis Results

For the worst-case MESSENGER orbital phase, the thermal radiator will periodically face directly to the Sun. At such times, the diode heatpipe will be automatically switched off to avoid conducting heat back into the box. The entire IEM will be in a 'self-heating' mode for approximately 40-minutes per orbit.

In order to approve the IEM thermal design in the worst-case transient condition, self-heating transient analyses have been conducted. The heatpipe temperature was predicted to be 34°C at the beginning of self-heating by the spacecraft thermal model. Steady-state thermal analysis was conducted at that boundary condition, and the instantaneous temperature distribution in the IEM was used as the initial condition for the transient thermal analysis. The IEM was then kept isothermally with its own thermal mass to absorb the power dissipation. It was discovered from the analyses that radiation among the PWBs must be taken into account. Figure 14 is a plot of the RAD6000 temperature as a function of time during self-heating, including the effect of radiation from the PWBs. The transient analyses have proven that

the thermal design meets all the requirements even in worst-case orbits.

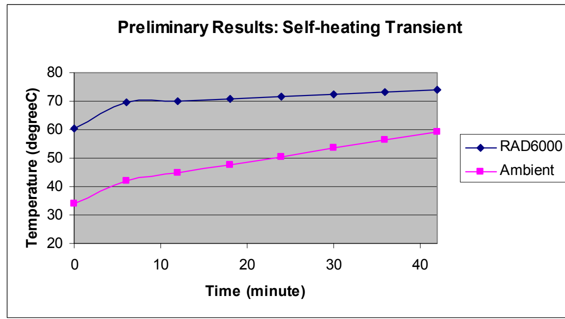

Figure 14: Transient Thermal Analysis Results

MESSENGER IEM Structural Design

The lightweight structure is achieved by using a thin-wall aluminum chassis designed to meet the stringent mass budget for the MESSENGER mission. However, the lightweight IEM housing needs to be mechanically effective in providing adequate structural support to the PWBs and the electronics during launch and throughout the entire mission. It is expected that the thin wall chassis, its slim footprint, and the relatively tall structure can result in a reduced first-mode chassis frequency, so extra care has been taken to tailor the board frequencies to be distinct from the chassis frequencies to avoid resonances.

IEM Dynamics Analysis

Detailed structural analyses were performed on the PWBs and the complete IEM chassis assembly. The PWB's first natural frequency must be above 150 Hz to avoid significant coupling with the spacecraft main structure, and the chassis's first natural frequency must be separate from the first-mode frequency of the board to decrease the transmissivity of the dynamics loads from the chassis to the board.

Stiffeners are used in the MP, the FPP, and the interface board designs to increase the overall stiffness of the PWB. The SSR has an aluminum frame (2.54 mm) sandwiched between two single-sided PWBs, designed mainly to address thermal concern with the plastic SDRAMs on the SSR board, but providing strength to the PWB structure at the same time. The DC-DC converter board has an AlBeMet heatsink plate (2.03 mm) bonded on the secondary side of the PWB, assisting dissipation of the concentrated converter power, while supporting the relatively heavy weight of the converters.

The SSR board, subcontracted to BAE Systems, incorporates a Ceramic Column Grid Array (CCGA) package on the board. The package is fairly large (32x32 mm) and has 624 pins, which results in a significant amount of stress accumulation among the solder joint interconnections due to the CTE (Coefficient of Thermal Expansion) mismatch between the ceramic package and the polyimide PWB. BAE leverages the compliance of the tall, slim solder columns to absorb the thermally induced mechanical stress, increasing the fatigue life of the package. The structural analysis for the SSR board has been performed to ensure that all the components, including the CCGA package, will survive the vibration loads, and to demonstrate the sufficient fatigue life for the assembly. Figure 15 shows the finite element model of the SSR board and the analysis results. The board is simply supported at the top and bottom wedgelock sides, as well as on the front side. It is simply supported at the locations where the backplane connectors are located. As it can be seen from the results, the frequency and the deflection of the SSR board meet the structural requirements of the MESSENGER mission.

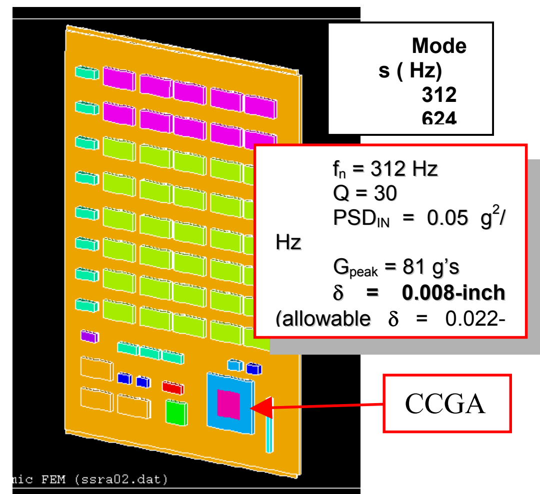

Figure 15: Dynamic Analysis Finite Element Model and Results

IEM Pre-engineering Vibration Test

Vibration tests, using a pre-engineering chassis and dummy PWBs, as shown in Figure 16, were conducted to verify the structural design and prove the concept of the slip-joint mounting. The CCGA was populated on the SSR board, and electrical connectivity of the solder columns was monitored using the daisy-chained design. The connectivity of the Compact PCI backplane connectors was also monitored during the test. The test specifications [6] with doubled duration of random vibration for margin, are as follows:

Sine Vibration Levels: Thrust Axis (X)

Frequency (Hz)	Acceleration
5 – 7.4	0.5 in. (double amplitude)
7.4 – 23	1.4 g
25 – 27	16 g
29 – 100	1.4 g

Rate = 4 Octaves/min

Sine Vibration Levels: Lateral Axis (Y, Z)

Frequency (Hz)	Acceleration
5 - 6.3	0.5 in. (double amplitude)
6.3 – 19	1.0 g
21 - 23	12 g
25 – 100	1.0 g

Rate = 4 Octaves/min

Random Vibration Levels: Normal to the Mounting Plane (Z)

Frequency (Hz)	PSD (g^2/Hz)
20	0.0063
20 – 80	+6.0 dB/oct
80 – 800	0.1
800 – 2000	-9.0 dB/oct
2000	0.0065

Overall Amplitude = 10.4 Grms
Duration = 120 s

Random Vibration Levels: Axes in the Mounting Plane (X, Y)

Frequency (Hz)	PSD (g^2/Hz)
20	0.0031
20 – 80	+6.0 dB/oct
80 – 800	0.05
800 – 2000	-9.0 dB/oct
2000	0.0032

Overall Amplitude = 7.4 Grms
Duration = 120 s

Figure 16: Dummy PWB Boards for the IEM Pre-engineering Vibration Test

The vibration tests were conducted on an electrodynamic shaker, as shown in Figure 17. The board frequencies are monitored using 'tear drop' uniaxial accelerometers attached to each PWB, and the chassis dynamics response is monitored by tri-axial accelerometers.

Vibration tests were conducted according to the following sequence, for all three axes:

- Pre sine survey: 5-2000 Hz at 0.5 g
- Random vibration 3 dB lower per given specification
- Sine vibration per given specification
- Post sine survey: 5-2000 Hz at 0.5 g

- First inspecting the mounting brackets, checking for any residual indicating relative slippage of the washers against chassis brackets.

- Random vibration per given specification

- Second inspecting the mounting brackets, checking for any residual indicating relative slippage of the washers against chassis brackets.

Test results for the CCGA integrity and Compact PCI backplane connector connectivity are promising. There have been no intermittent effects or openings observed for any of the tests. Table 2 lists the first natural frequency of the IEM chassis and all the PWBs. The structural design has successfully reduced resonant effects and has isolated the PWBs from chassis vibration.

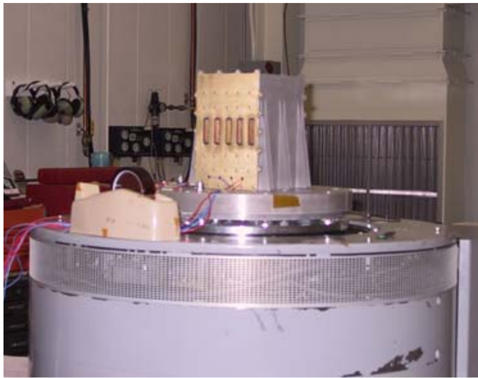

Figure 17: IEM Pre-engineering Model on the Shaker for Vibration Tests

Table 2: First Mode Frequency of the IEM

	Frequency (Hz)
IEM Assembly	250
DC-DC converter board	380
SSR	380
MP	320
Interface	300
FPP	350

Several observations were made during the tests, which prompted further investigation of the slip-joint mounting scheme.

1) It is difficult to align the stack of washers, especially those on the bottom of the mounting foot, even with spot faces at the bottom of the mounting brackets.

2) Black residual material observed on the washers and mounting foot suggested that relative slippage occurred during the vibration. In several washers, the NEDOX coating was scratched off due to the slippage.

3) There were marks of indentation, suggesting that the given torque value was too high, that the thin, coated washers were 'pushed' into the mounting holes.

A modified slip-joint scheme is under development. More washer-coating tests are underway to determine the coefficient of friction. Thicker washers are being considered to increase structural stability, and further vibration tests are planned to validate modified design.

Conclusion

Thermal analysis, structural analysis, and tests proved the feasibility and integrity of the design for the Integrated Electrics Module for the MESSENGER spacecraft. The thin-wall aluminum chassis design reduced overall weight. The slip-joint mounting configuration is still undergoing further development, testing, and validation.

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